# CS 330 Homework 4-A

These questions refer to Figure 4.11 on page 258 of the text. That diagram shows some different parts of our MIPS processor implementation. In your answers to these questions, refer to them by these names:

- Instruction memory
- Data memory
- Register file
- Sign extend unit
- Shift-left 2 unit
- ALU (the full-capability ALU located between the Register file and Data memory)
- Add PC + 4 unit (located in upper-left of diagram)
- Add (shift-left 2) + (PC + 4) unit (located in upper-right of diagram)

1. Determine which parts of the processor are used when executing each of the following instructions.
   (a) `add  $t0, $t1, $t2`
   (b) `addi $s0, $s1, -1`
   (c) `beq $sp, $gp, reboot_code` (Assume the branch does not take place.)
   (d) `bne $t0, $t1, loop_begin` (Assume the branch takes place.)
   (e) `slt $t0, $s0, $zero`
   (f) `sw $t0, 1024($s0)`
2. Suppose the processor is performing the instruction `add $t0, $t1, $t2`.
   (a) Which input should the `ALUSrc` mux select: Read data 2, Sign extension unit, or is this a don't care?
   (b) Which input should the `MemtoReg` mux select: Read data, ALU Result, or is this a don't care?
   (c) Which input should the `PCSrc` mux select: Add-4 ALU, Add-shift-left-2 ALU, or is this a don't care?
3. Suppose the processor is performing the instruction `lw $t0, -4($s0)`.
   (a) Which input should the `ALUSrc` mux select: Read data 2, Sign extension unit, or is this a don't care?
   (b) Which input should the `MemtoReg` mux select: Read data, ALU Result, or is this a don't care?

(c) Which input should the `PCSrc` mux select: Add-4 ALU, Add-shift-left-2 ALU, or is this a don't care?

4. Suppose the processor is performing the instruction `bne $a0, $zero, loop`.

   (a) Which input should the `ALUSrc` mux select: Read data 2, Sign extension unit, or is this a don't care?

   (b) Which input should the `MemtoReg` mux select: Read data, ALU Result, or is this a don't care?

   (c) Which input should the `PCSrc` mux select: Add-4 ALU, Add-shift-left-2 ALU, or is this a don't care?

5. Why do you think a single-cycle MIPS datapath must have separate instruction and data memories. (Hint: Consider the entire fetch-execute-decode cycle for an instruction like `lw $s1, 0($s0)`. What actions must the processor perform in one clock-cycle when executing this instruction.)