CS 330 Homework 4-B

1. Processor designers want to make the clock speed as high as possible.

   (a) Why?

   (b) Since clock speed is the reciprocal of the clock rate, we could also state that designers want to make the clock cycle time as small as possible. What determines the smallest possible clock cycle time in a non-pipelined processor?

   (c) What determines the smallest possible clock cycle time in a pipelined processor?

2. A processor contains three functional units. The units and the time required for each unit to perform its function are listed below.

   Unit 1: Instruction fetch and decode, 200 ps.

   Unit 2: Operand fetch and instruction execution, 300 ps.

   Unit 3: Store instruction result, 150 ps.

   (a) What is the clock cycle time of a single-cycle implementation of this processor?

   Suppose that we reimplement the processor, placing each unit in a pipeline stage. The times of each stage are unchanged.

   (b) Does this pipeline have balanced or unbalanced stages?

   (c) What is the smallest possible clock cycle time of the pipelined processor?

   (d) Suppose that you can split one stage of the pipeline datapath into two new stages, each of which uses 1/2 of the time of the original stage.

      i. What stage would you split?

      ii. What is the new clock cycle time of the processor?

3. Draw a diagram similar to figure 4.28 of the text that shows the instruction pipeline for the instruction `beq $s0, $s1, offset`. Use shading to indicate whether each stage is used at the beginning of the clock cycle, the end of the cycle, the entire cycle, or is not used during instruction execution.